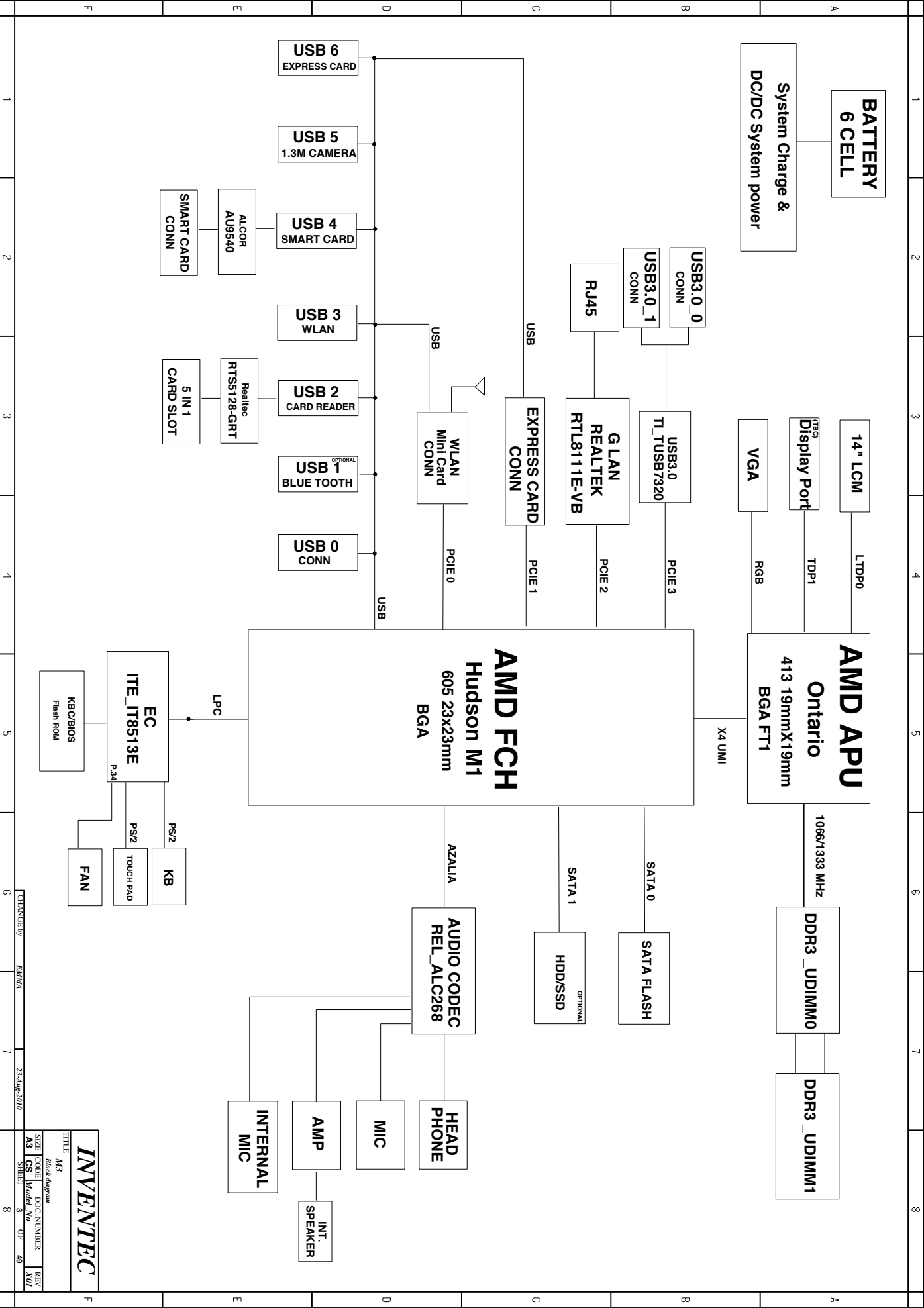
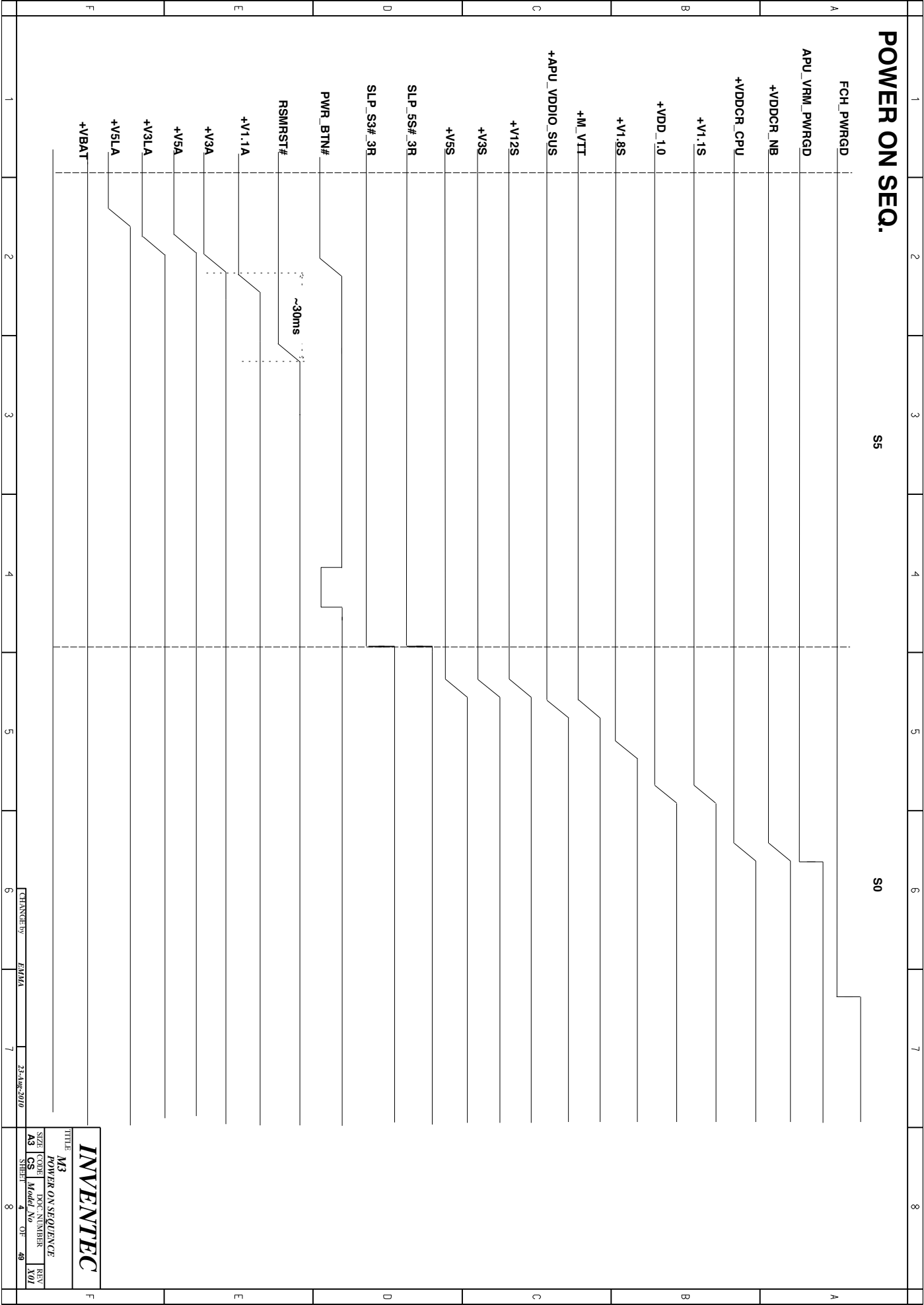


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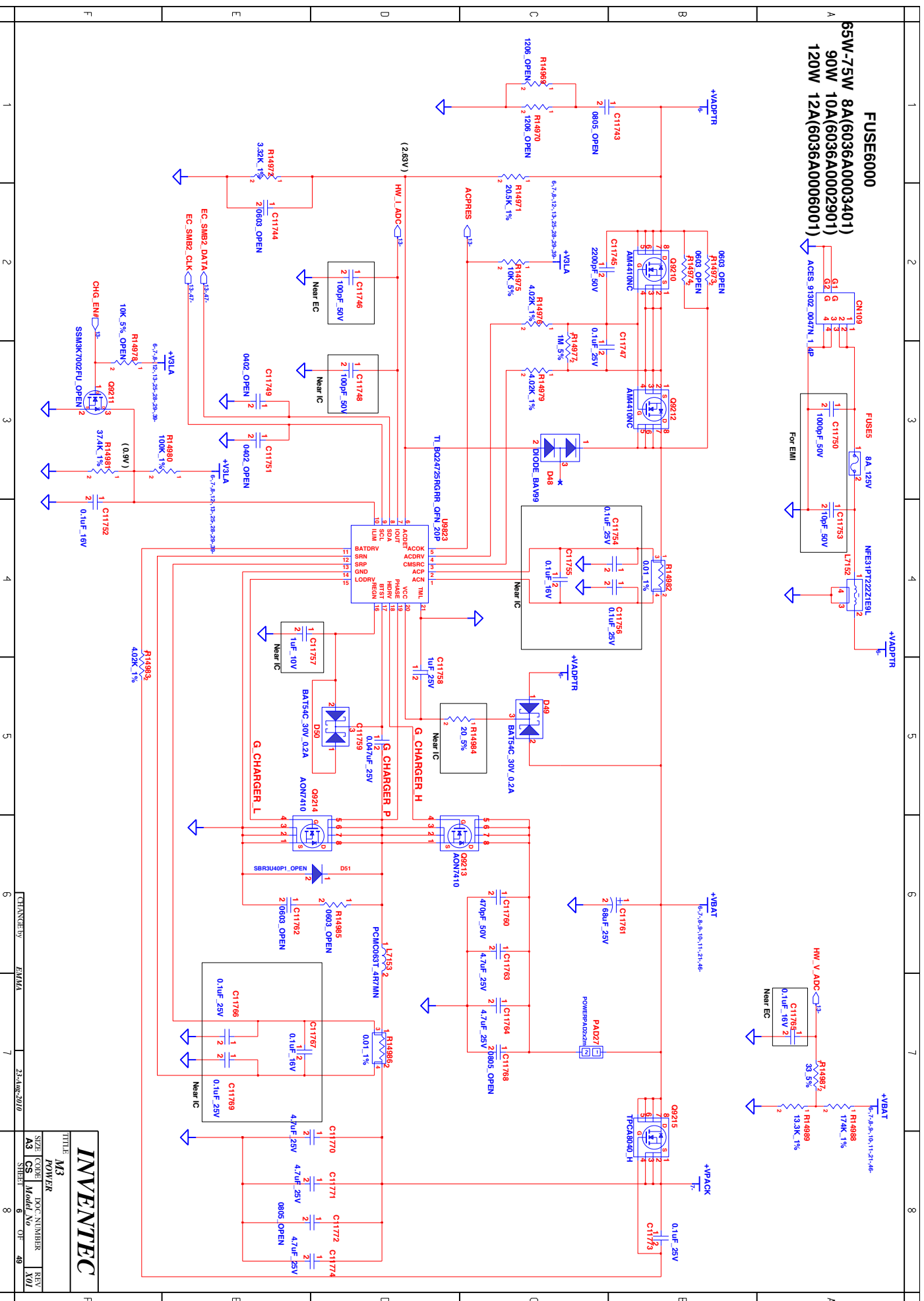
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SIZE		CODE	DWG NUMBER		REV																					
A3		CS	Model No.		X01																					
SHEET		1		OF		49																				
<table><tr><td>DR/WR</td><td>SE</td><td>DATE</td><td>POWER</td><td>DATE</td></tr><tr><td>DESIGN</td><td></td><td></td><td></td><td></td></tr><tr><td>CHECK</td><td></td><td></td><td></td><td></td></tr><tr><td>RESPONSIBLE</td><td></td><td></td><td></td><td></td></tr></table>							DR/WR	SE	DATE	POWER	DATE	DESIGN					CHECK					RESPONSIBLE				
DR/WR	SE	DATE	POWER	DATE																						
DESIGN																										
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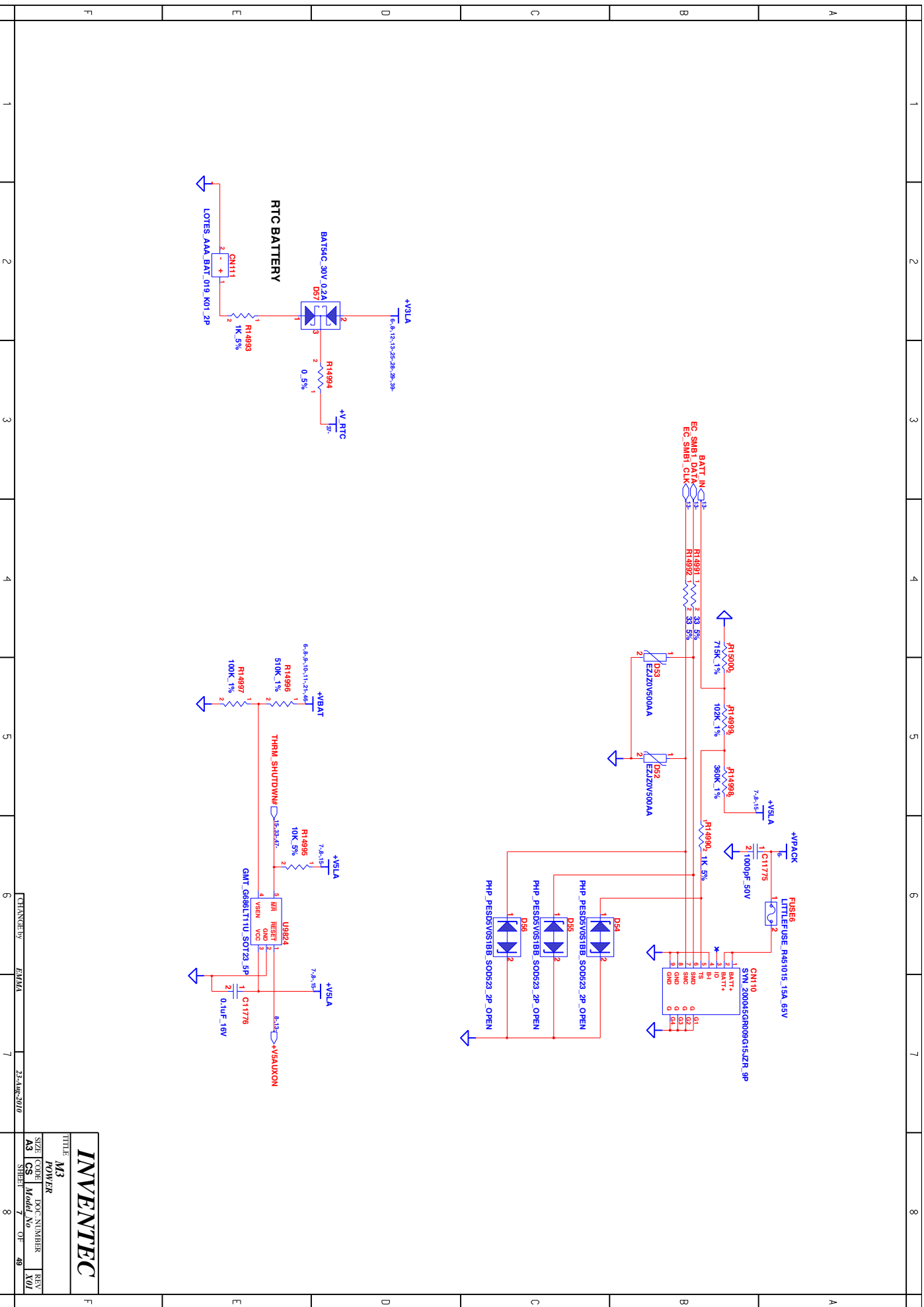
	1	2	3	4	5	6	7	8	
A	<div>TABLE OF CONTENTS</div>								
B	<div> <div>PAGE</div> <div> 1. COVER PAGE 2. INDEX 3. BLOCK DIAGRAM 4. POWER ON SEQUENCE 5-13. RESERVE FOR SYSTEM POWER 14. APU FT1 1 15. APU FT1 2 16. APU FT1 3 17. APU FT1 4 18. DDR SO-DIMM 19. FCH1 20. FCH2 21. FCH3 22. FCH4 23. STRAP OPTION / THERMAL / RTC 24. DVI-I 25. DVI-D 26. WLAN / BT 27. TPM </div> </div>								
C	<div> <div>PAGE</div> <div> 28. SATA FLASH CONN 29. CODEC REL_ALC268 30. AMP / INT. SPEAKER 31. SMART CARD AU9540 32. GIGA LAN 33. RJ45 / DUAL USB 34. IT8712 35. SERIAL / PARALLEL CONN 36. PS/2 CONN 37. USB3.0 CONTROLLER 38. DUAL USB3.0 CONN / PIN HEADER 39. USB CONN 40. AUDIO JACK / POWER SW 41. RISER CARD </div> </div>								
D									
E									
F	<div> <div> <div>1</div> <div>2</div> <div>3</div> <div>4</div> <div>5</div> <div>6</div> <div>7</div> <div>8</div> </div> <div> <div>CHANGED BY</div> <div>REVIEW</div> <div>21-Aug-2010</div> </div> <div> <div> <div> <div>TITLE</div> <div>M3</div> </div> <div> <div>SIZE</div> <div>A3</div> </div> <div> <div>CODE</div> <div>CS</div> </div> <div> <div>DOC. NUMBER</div> <div>Model No</div> </div> <div> <div>REV</div> <div>X01</div> </div> </div> <div> <div> <div>INVENTEC</div> <div>index</div> </div> <div> <div> <div>2</div> <div>OF</div> </div> <div>49</div> </div> </div> </div> </div>								





	1	2	3	4	5	6	7	8
A								
B								
C								
D								
E								
F	<div><div>Power Block Diagram</div><div><div><div>TITLEM3POWER SIZE CODEDOC NUMBERREV A3CSAdd NoX01 SHEET3OF49</div><div>INVENTEC</div></div><div>CHANGE BYEJMA23-Aug-2010</div></div></div>							





INVENTEC

M3

POWER

SIZE CODE DOC NUMBER REV

A3 CS Model No X01

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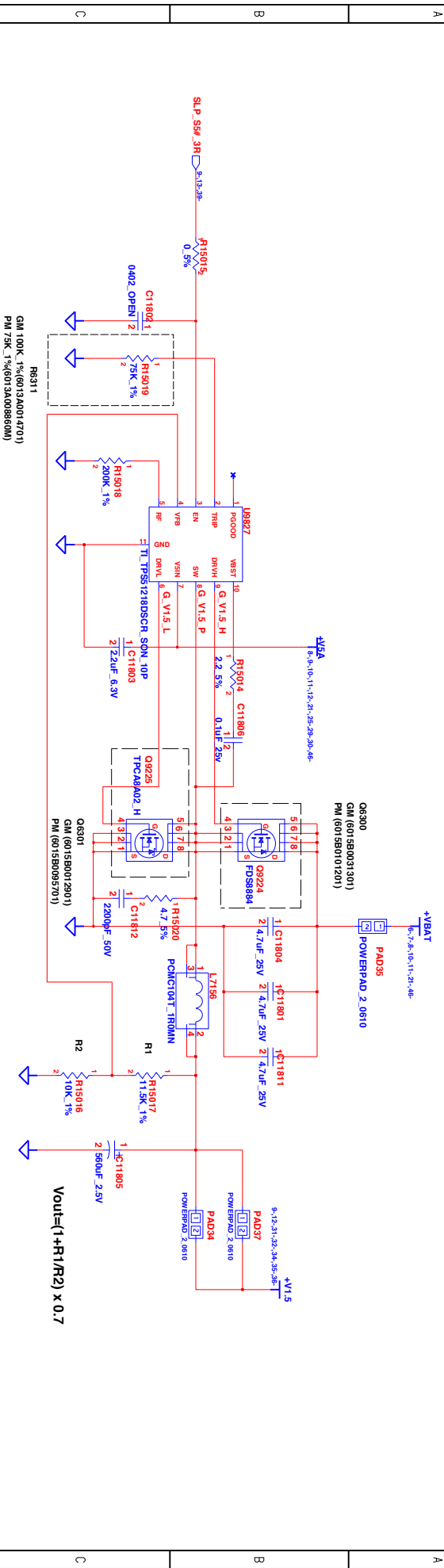
21-Aug-2010

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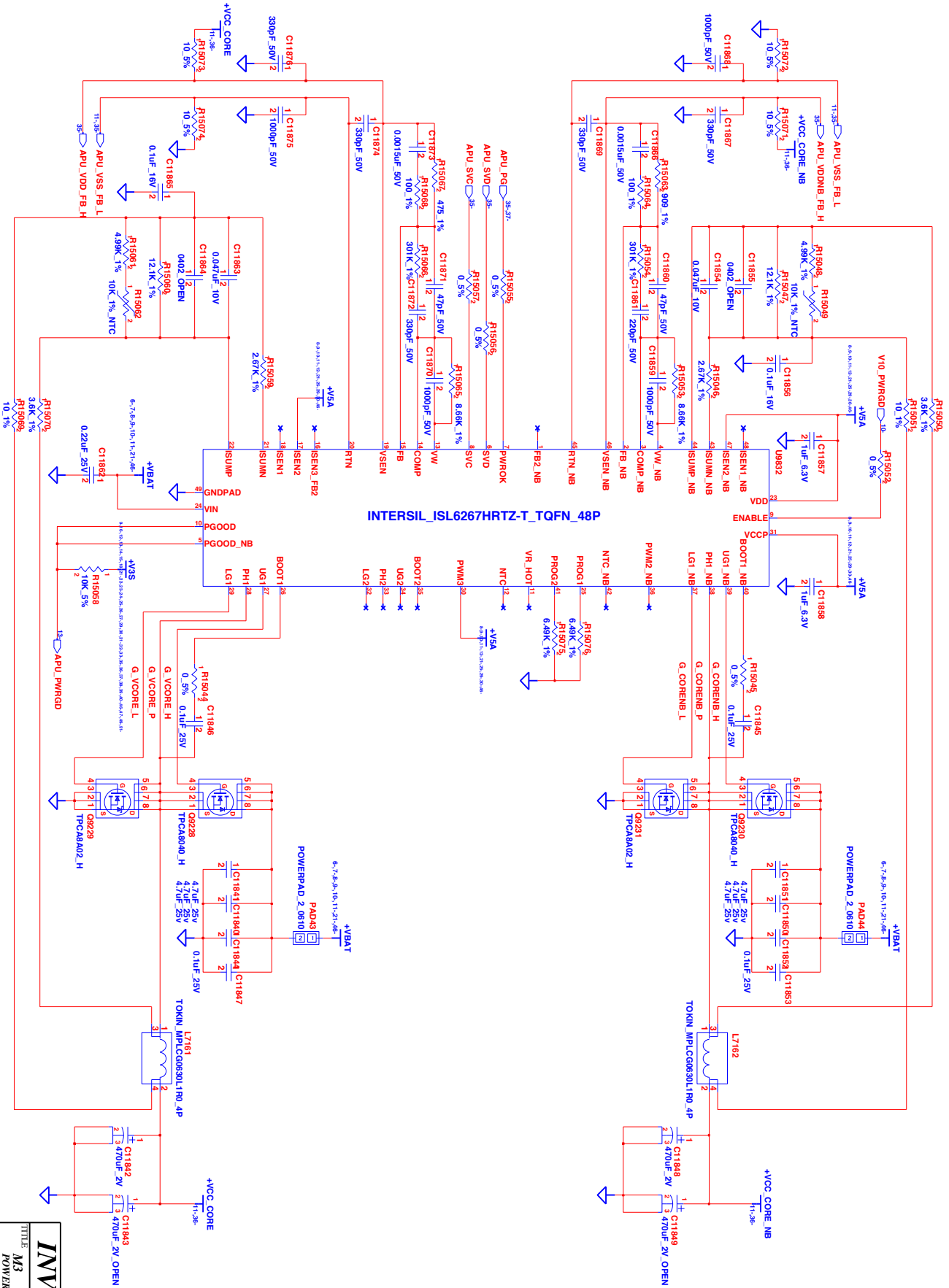
TITLE
M3
POWER

SIZE	CODE	DOC. NUMBER	R
A3	CS	Model No	X
SHEET 8 OF 49			

The schematic diagram illustrates a 12VDC to 5VDC buck converter. The input is a 12VDC source (V12A) connected to the SW pin of the MOSFET (IRF540). The MOSFET's gate is driven by a 5VDC source (V1.5B) through a 10kΩ resistor (R1). The MOSFET's drain is connected to the inductor (L1), which is in series with the output capacitor (C1) and the load. The inductor's other end is connected to the diode (1N5819) and the output filter capacitor (C2). The diode's cathode is connected to the MOSFET's source, which is grounded. The output voltage (Vout) is taken across the load resistor (R2) and is regulated by a feedback network consisting of resistors R1 and R2, and a capacitor C1. The output voltage is given by the formula: $V_{out} = (1 + R1/R2) \times 0.7$.



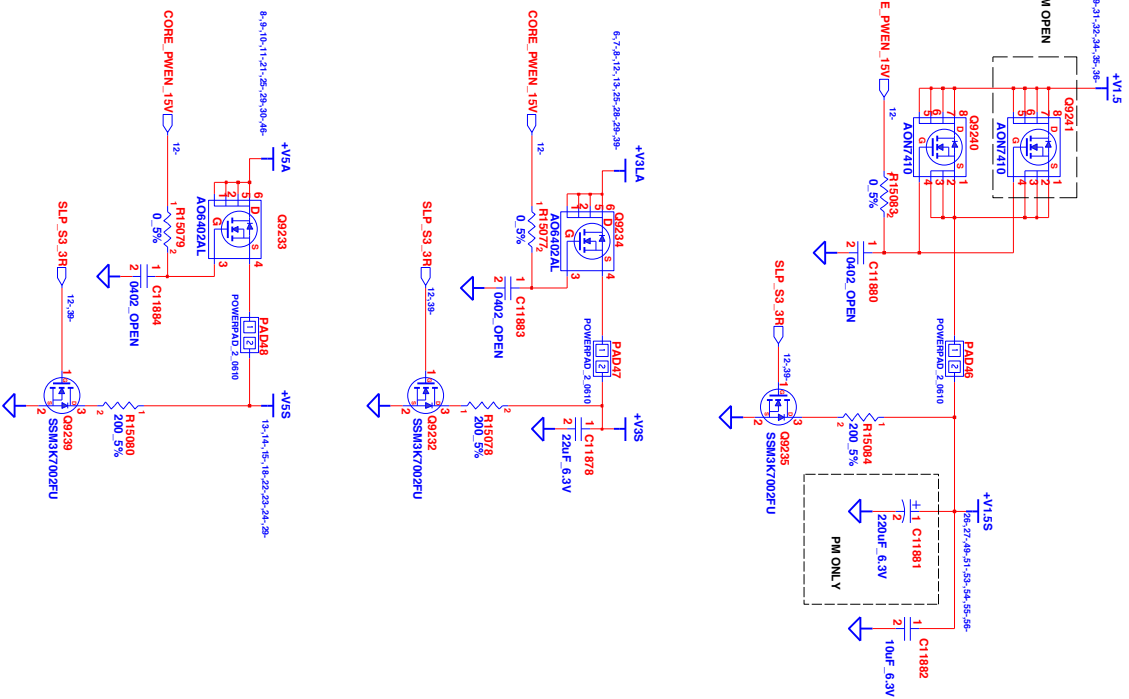
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TITLE M3		
POWER		
SIZE	CODE	DOC. NUMBER
A3	CS	<i>Model No</i>
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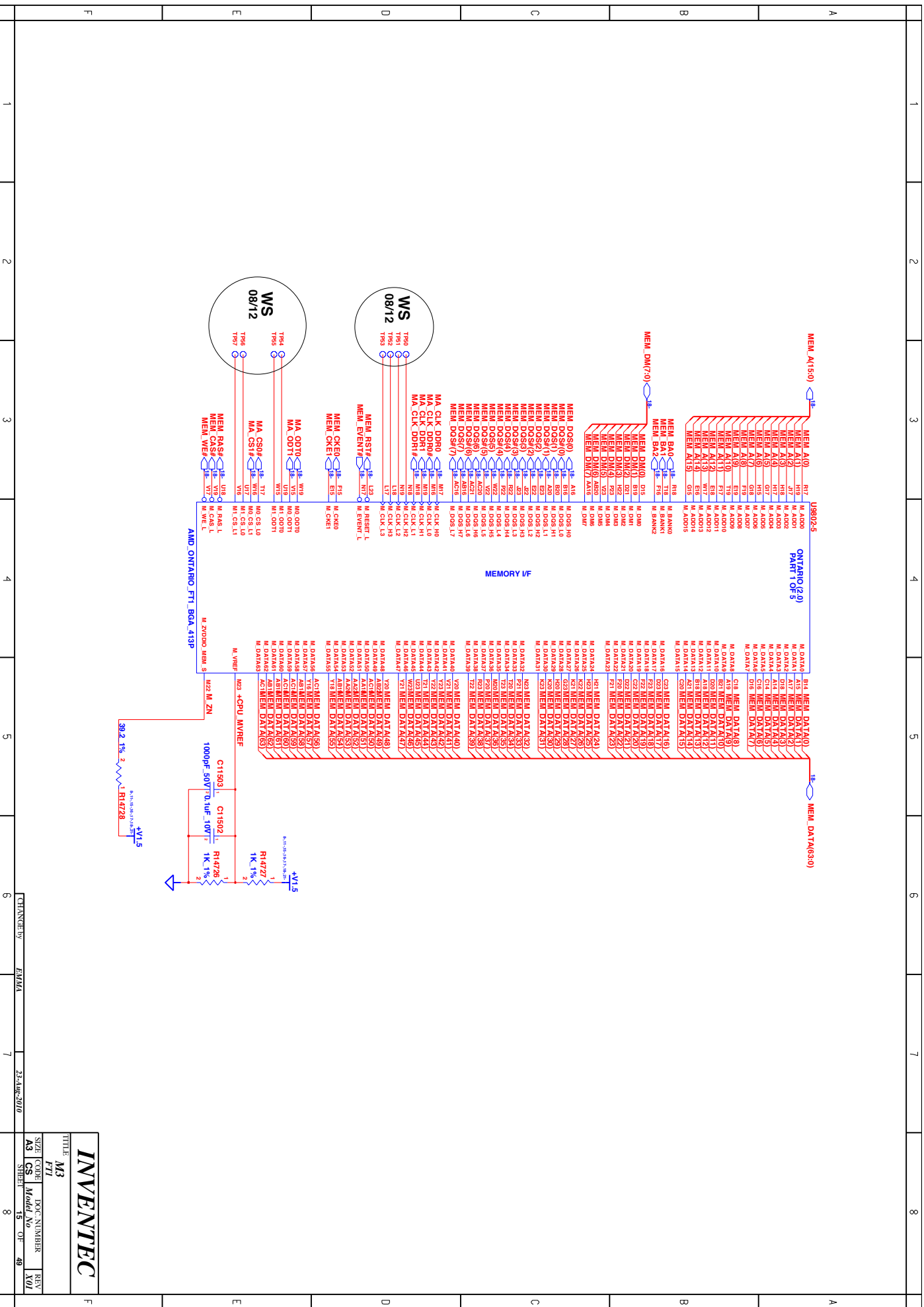


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INVENTEC			
TITLE			
M3			
POWER			
SIZE	CODE	DOC. NUMBER	REV.
A3	CS	Model. No	X01
SHEET		11	OF 49

9,10,11,13,14,15,18,21,22,23,24,25,26,27,29,30,31,32,33,35,36,37,38,39,40,46,47,49,51





INVENTEC

TITLE
M3

SIZE CODE
M3

REV
X01

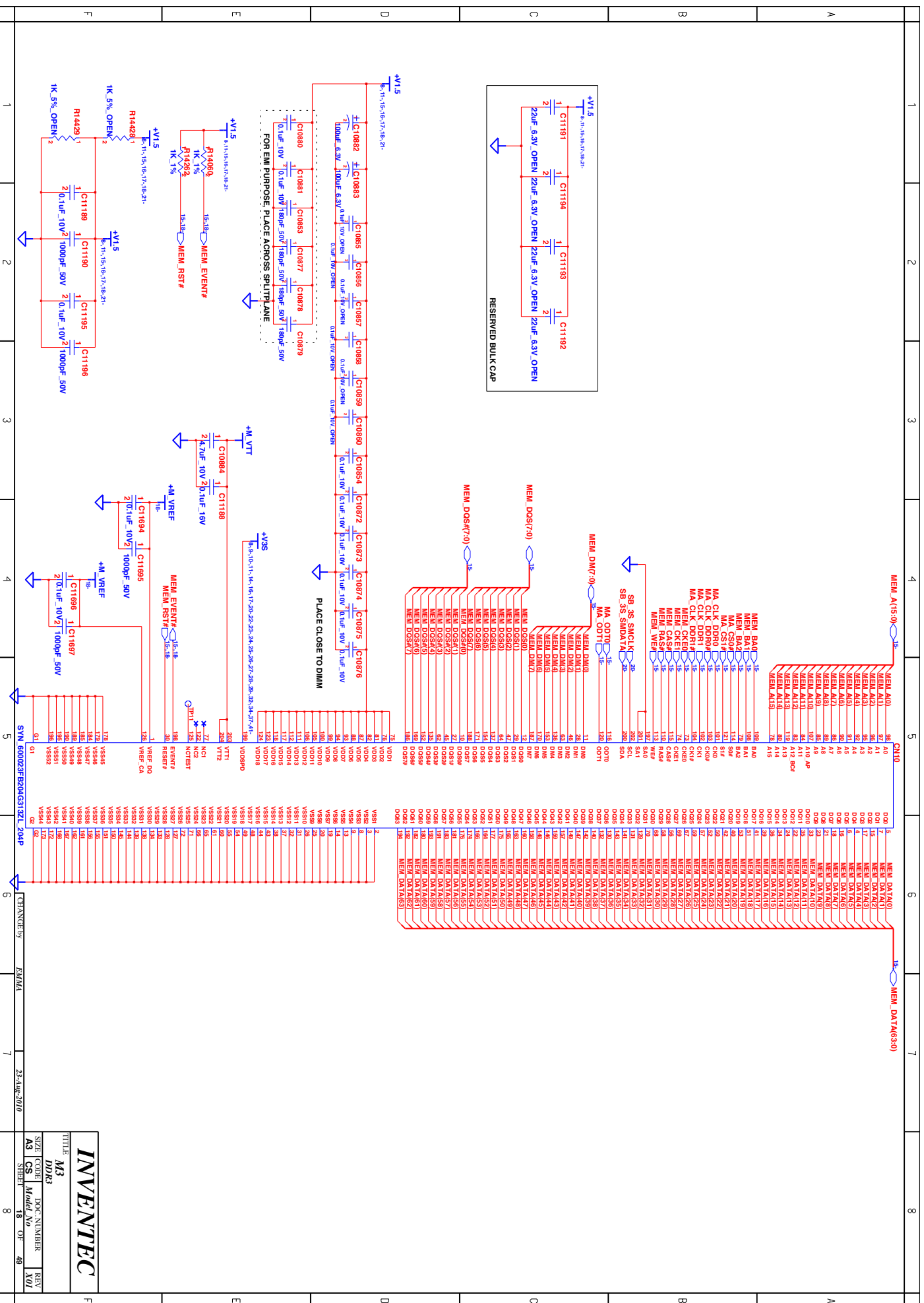
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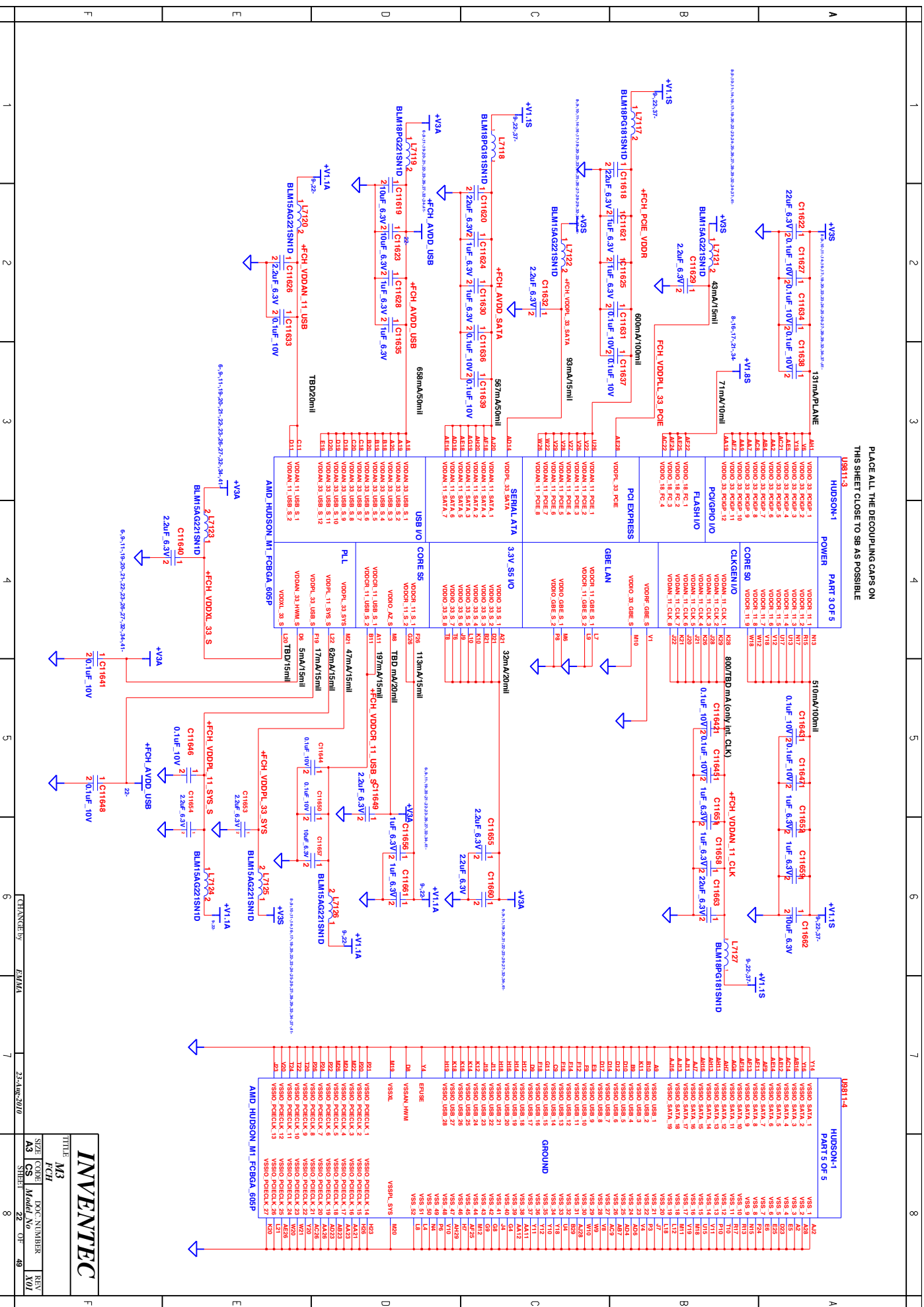
REV
49

CHANGED BY
HMA

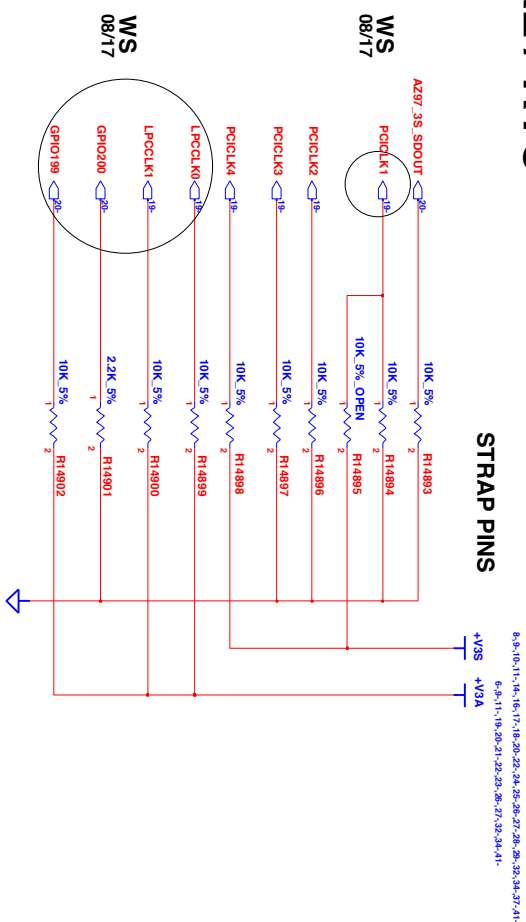
21-Aug-2010

8



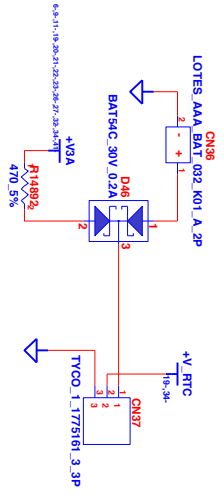


STRAP OPTION / THERMAL / RTC

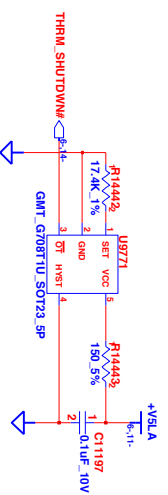


	AZ97_3S_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPCCCLK0	LPCCCLK1	GPIO200 EC_PWM3	GPIO199 EC_PWM2
PULL HIGH	Low Power Mode (Not Supported)	Allow PCIe Gen2	Watchdog Timer Enabled	Debug STRAP Enabled	Non-FUSION CLOCK Mode	Integrated Micro-Controller Enabled	Internal Clock Generator Enabled	H.H= Reserved H.L= SPIROM (Default)	
PULL LOW	Performance Mode (Default)	Force PCIe Gen1	Watchdog Timer Disabled	Debug STRAP Disabled	FUSION CLOCK Mode	Integrated Micro-Controller Disabled	Internal Clock Generator Disabled	L.H= LPC ROM L.L= Reserved	

RTC



Thermal Sensor



INVENTEC

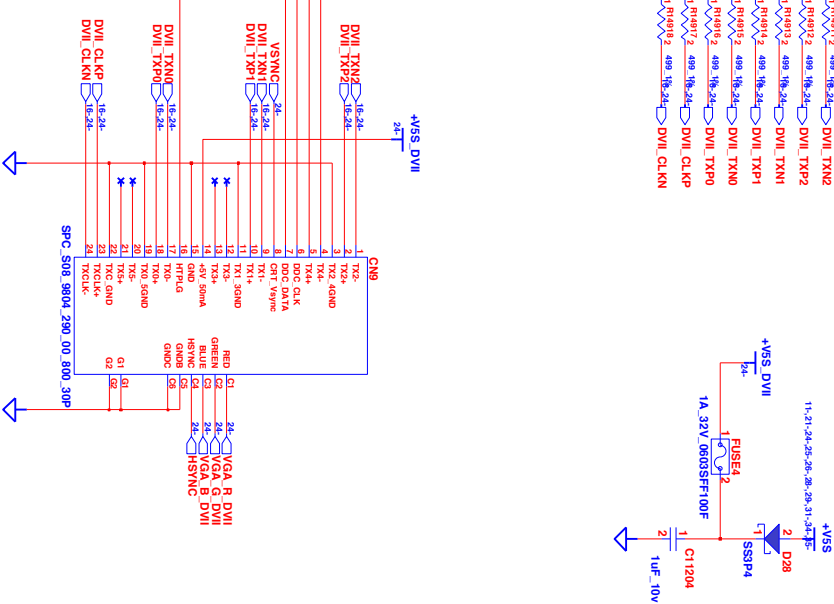
SIZE CODE

CS

REV

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Figure 1 illustrates the proposed VLSI architecture for the 2D-FFT algorithm. The architecture is divided into two main sections: **L7/8** and **L7/8**. The **L7/8** section contains six processing blocks, each receiving input from a **CRTR** buffer and outputting to a **VGA** buffer. The **L7/8** section contains six processing blocks, each receiving input from a **CRTR** buffer and outputting to a **VGA** buffer. The diagram also shows a series of control signals (**L7/8**, **L7/8**, **L7/8**, **L7/8**, **L7/8**, **L7/8**) and a series of data signals (**VGA**, **VGA**, **VGA**, **VGA**, **VGA**, **VGA**).

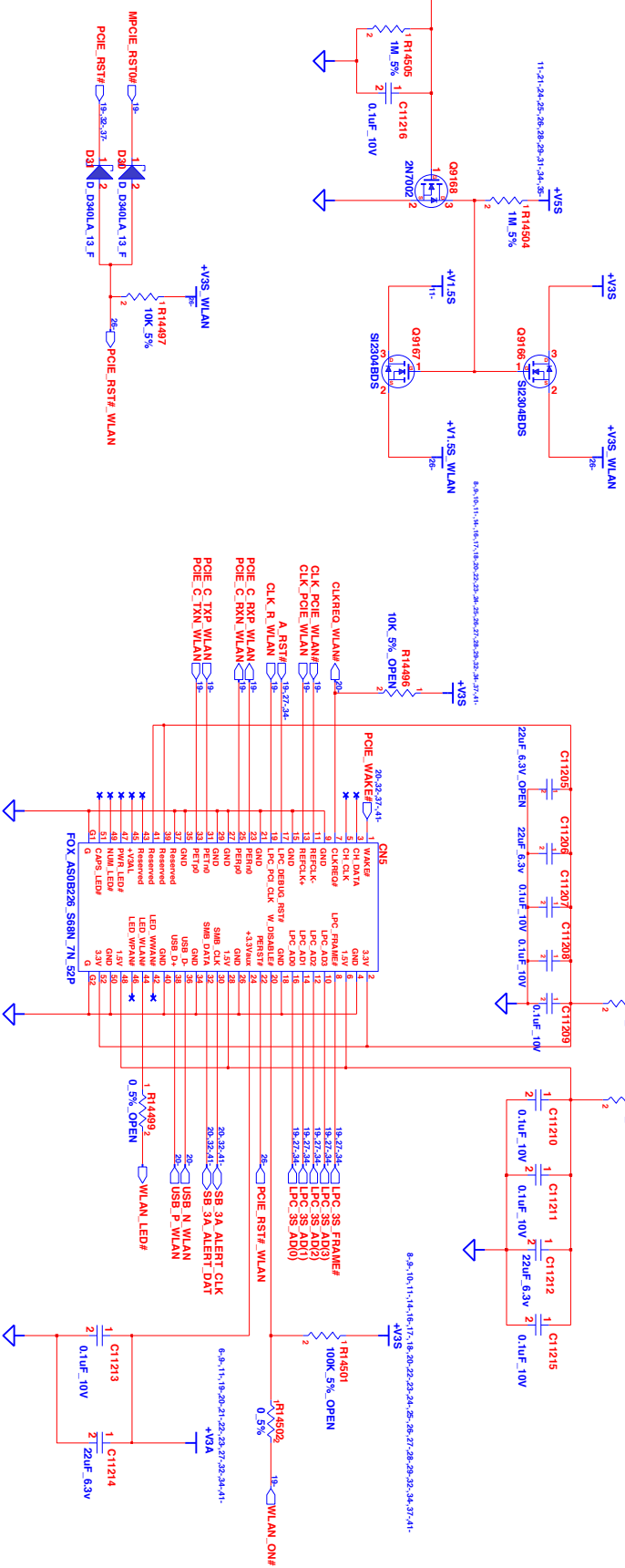


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TITLE			
<i>M3</i>			
<i>DVI-I</i>			
SIZE	CODE	DOC. NUMBER	REV
<i>A3</i>	<i>CS</i>	<i>Model No</i>	<i>X01</i>
SHEET		24	OF 49

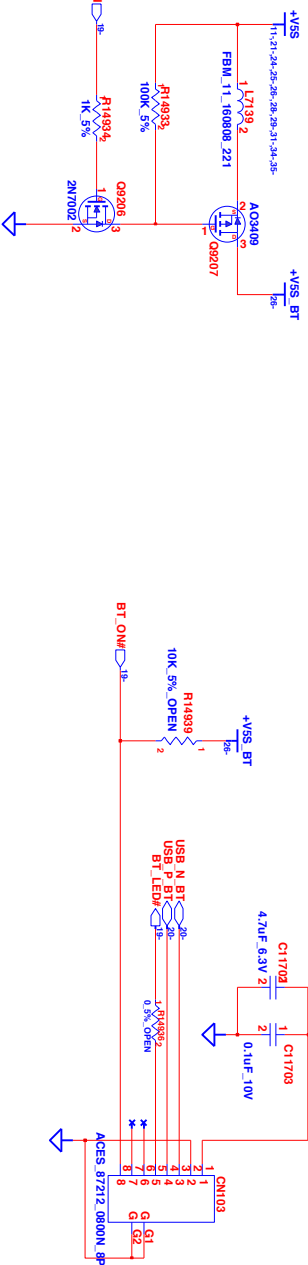


WLAN

MINI CARD CONN (WLAN)



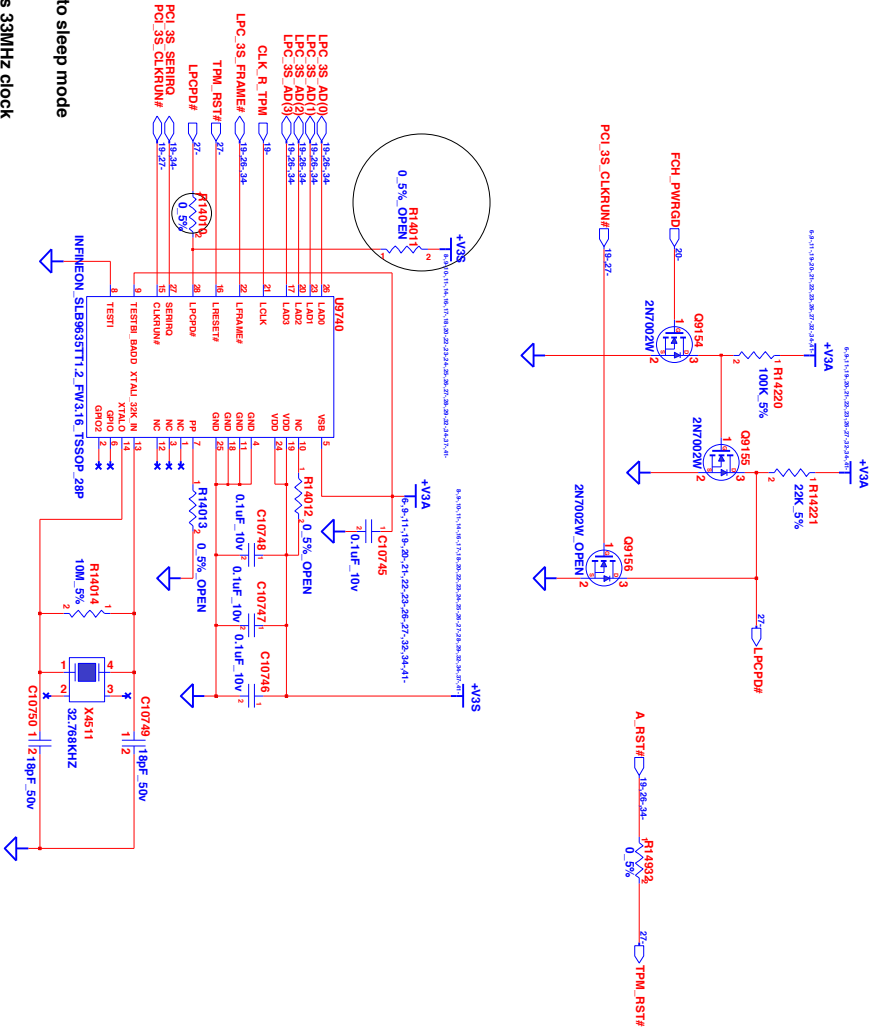
BT



INVENTEC			
TITLE: M3			
W/LAN /BT			
SIZE	CODE	DOC. NUMBER	REV.
A3	CS	Model No	X01
SHEET		26	OF 49

TPM

LPC_PWRDWN_L is used to force LPC peripherals to go into sleep mode
Device may require that this be asserted before entering S3
Device may require that this be asserted before stopping this 33MHz clock



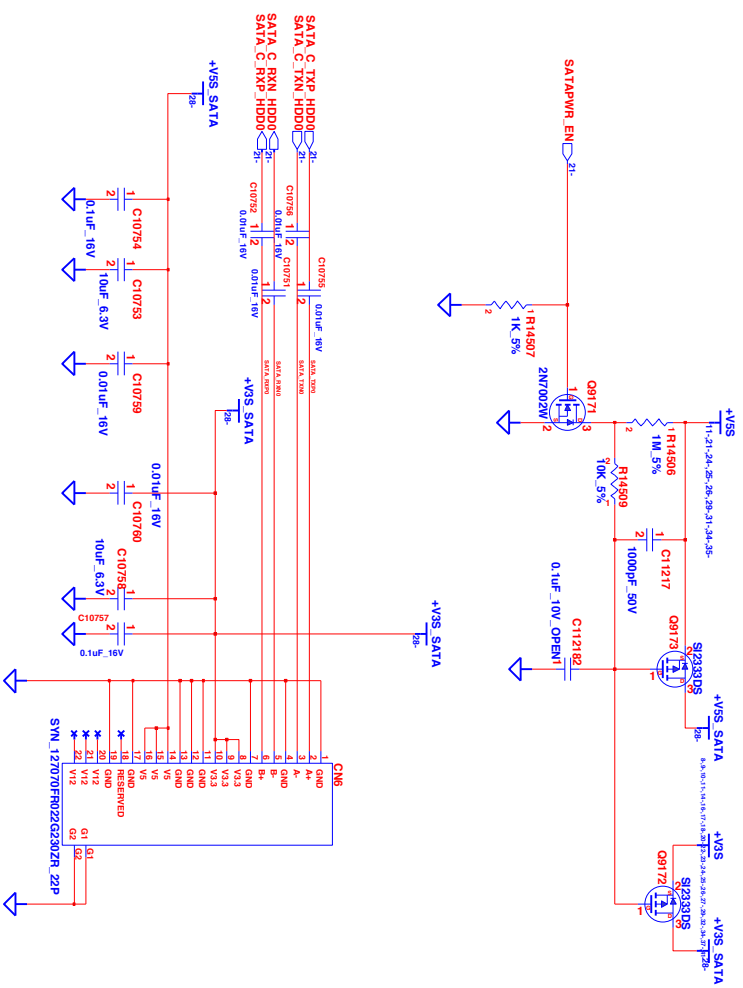
INVENTEC

SIZE CODE
M3

DOC NUMBER
REV

CS Model No
X01

SATA FLASH CONN.



SATA FLASH CONN.

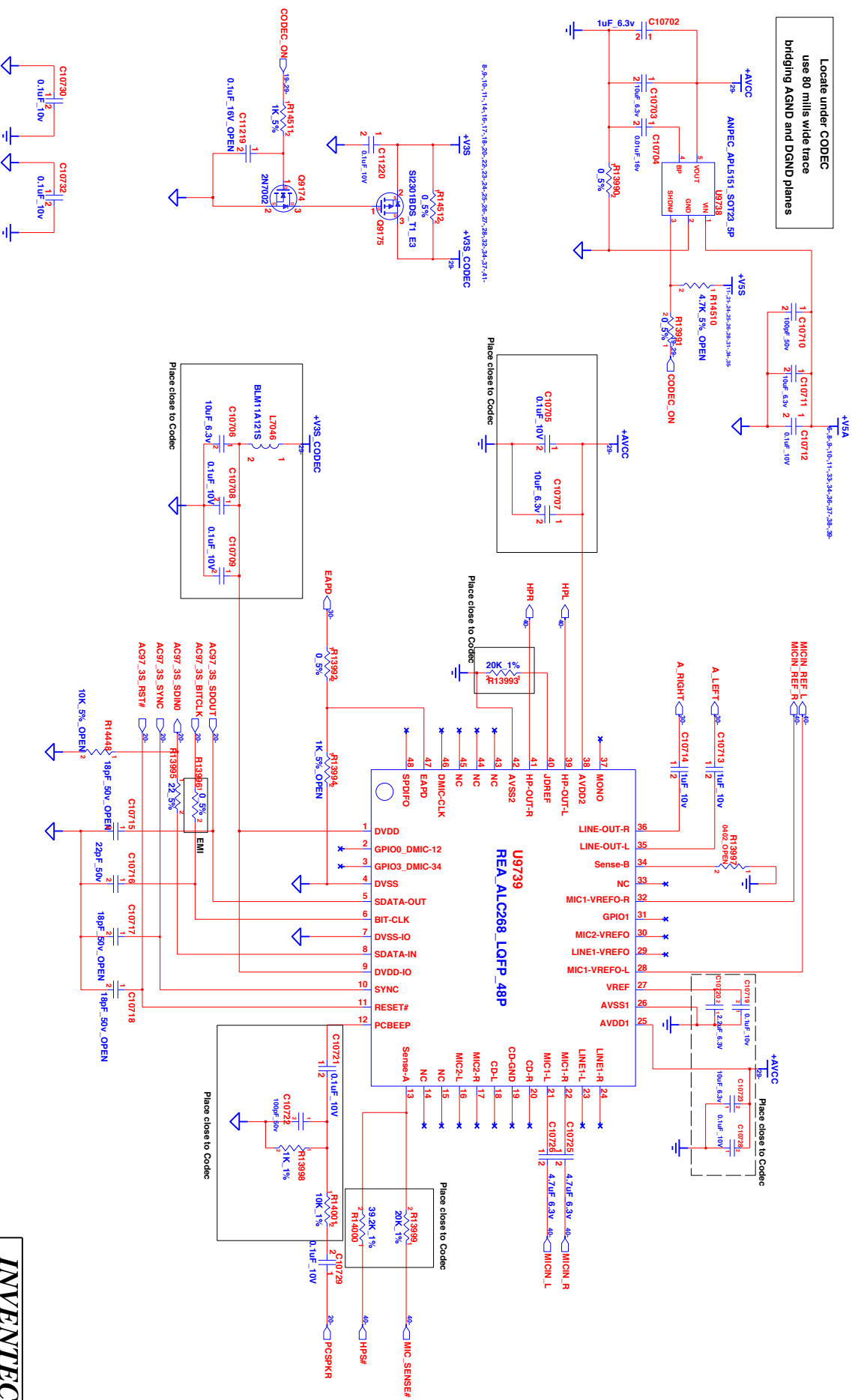
The schematic diagram illustrates the electrical connections for a SATA Flash Connector. It shows the interface between a SATA connector and a flash memory device. The connector pins are numbered 1 through 22, with pins 18 through 22 reserved. The diagram includes power and ground connections for +VSS SATA and -VSS SATA. Signal lines are connected to a flash memory device (SATA_FLASH). Key components include resistors (R14507, R14506, R14509), capacitors (C10752, C10754, C10753, C10759, C10756, C10757, C11217, C112182), and a SATA_PWR_EN signal. The diagram also shows the connection of SATA C TXP HDD0, SATA C TXN HDD0, SATA C RXN HDD0, and SATA C RXP HDD0 to the flash memory device.

TITLE		M3	
SATA FLASH CONN		REV	
A3		Model No	
SHEET		28	

INVENTEC		F	
SATA FLASH CONN		REV	
A3		Model No	
SHEET		28	

CODEC

Locate under CODEC
use 80 mills wide trace
bridging AGND and DGND planes



CHANGE by	EMMA	23-Aug-2010
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INVENTEC			
TITLE			
M3			
CODEC			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	<i>Model No</i>	X01
SHEET		29	OF 49

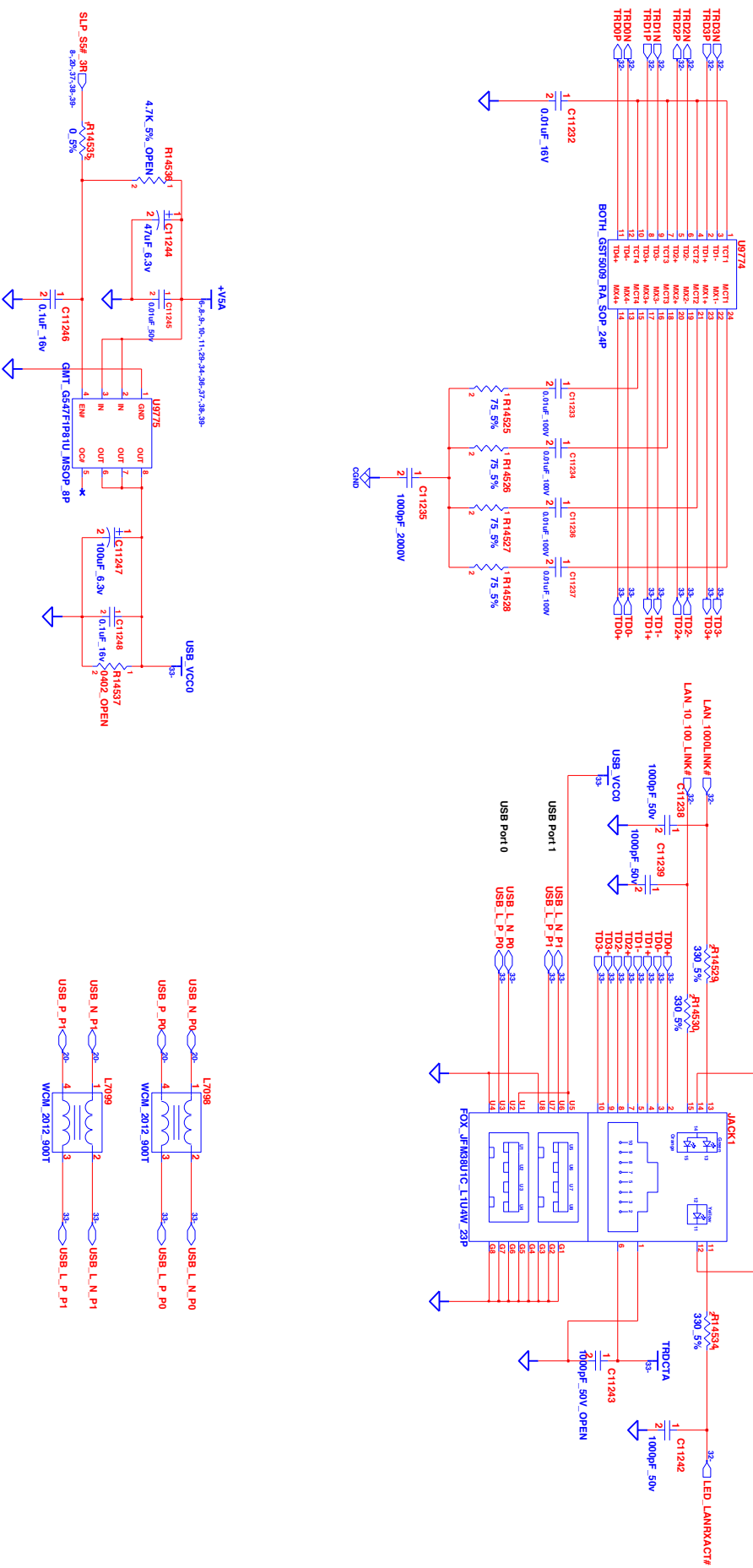
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SMART CARD

47

[illegible]

RJ45 / DUAL USB



INVENTEC

TITLE

M3

SIZE CODE

CS

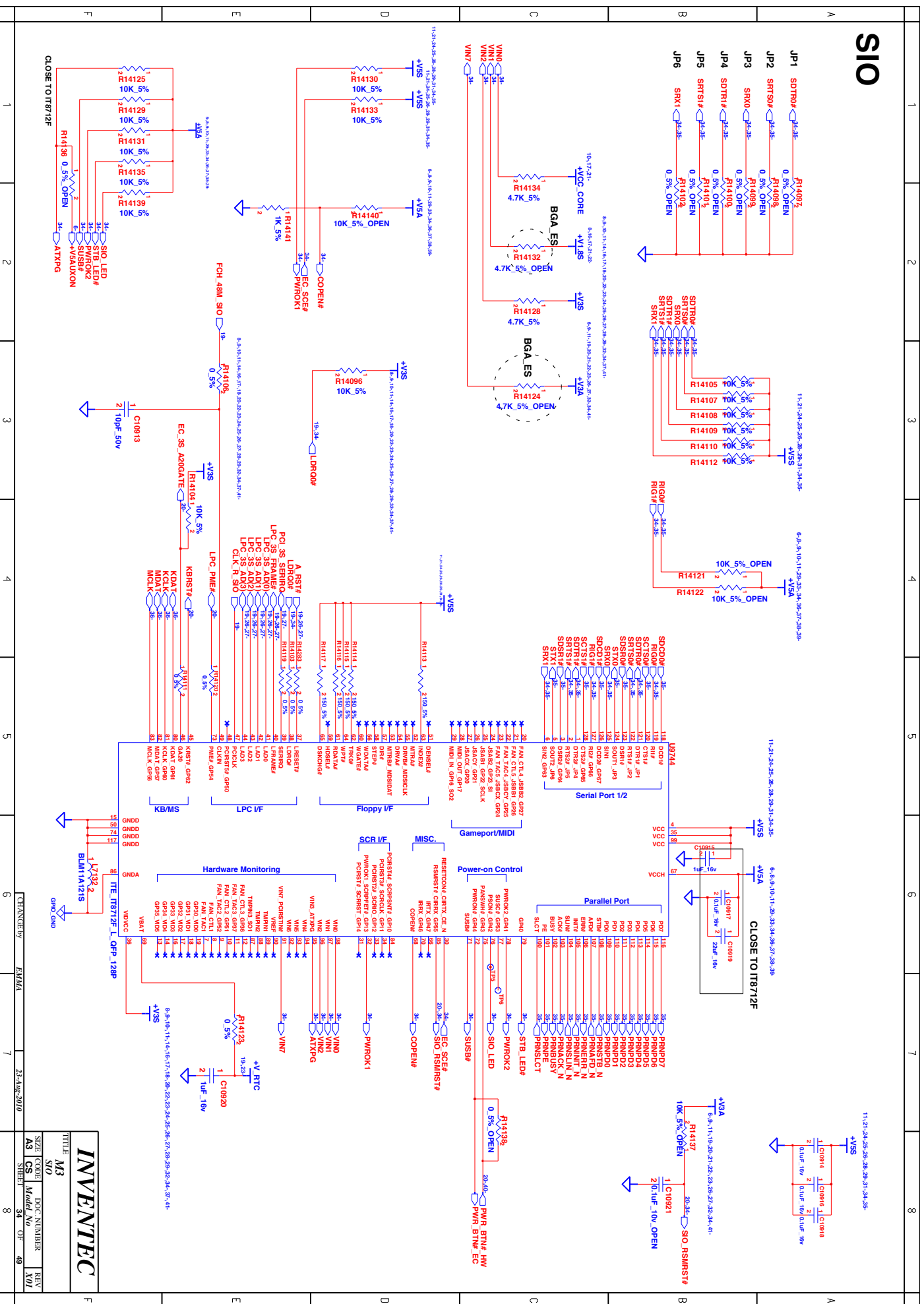
Model No

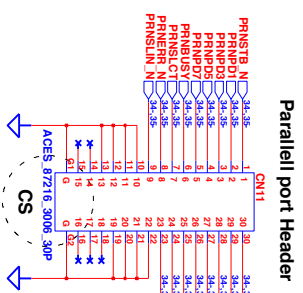
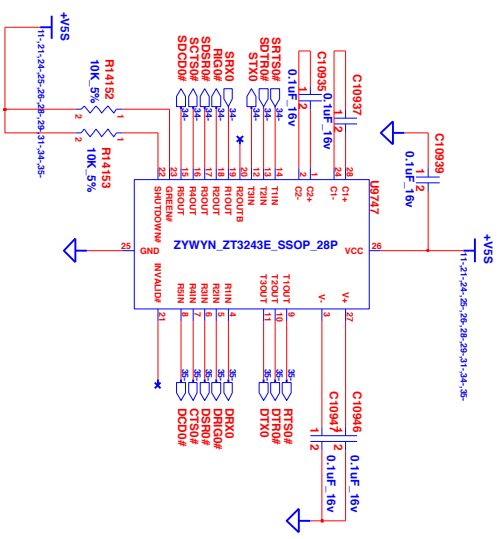
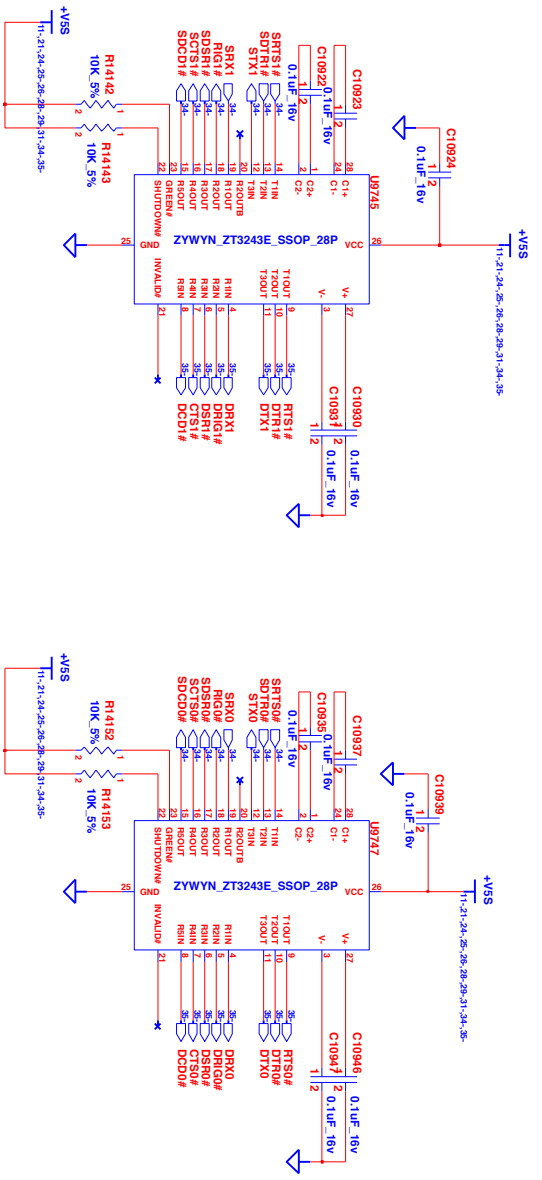
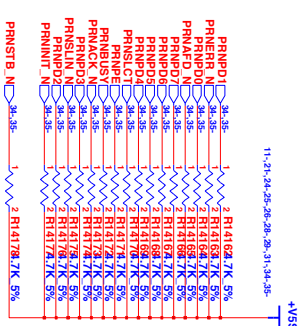
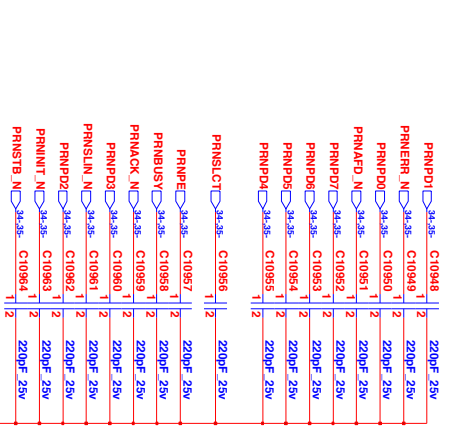
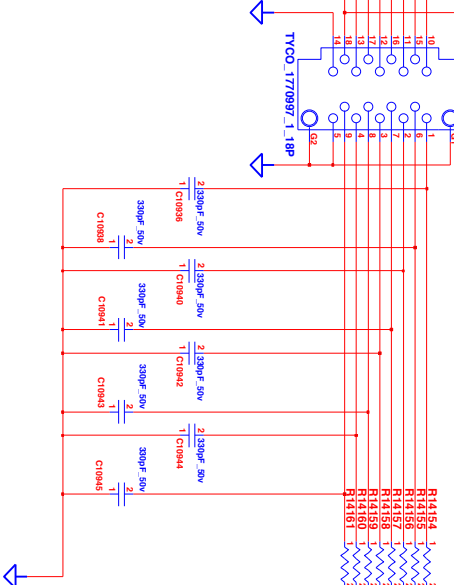
REV

33

OF

49





Note:

Cable	Header
2	1
4	2
6	3
8	4
5	5
7	6
9	7
10	8
12	9
14	10
16	11
18	12
15	13
17	14
21	15
20	16
22	17
24	18
26	19
28	20
30	21
	22
	23
	24
	25
	26
	27
	28
	29
	30

INVENTEC

M3

SERIAL/PARALLEL CONN.

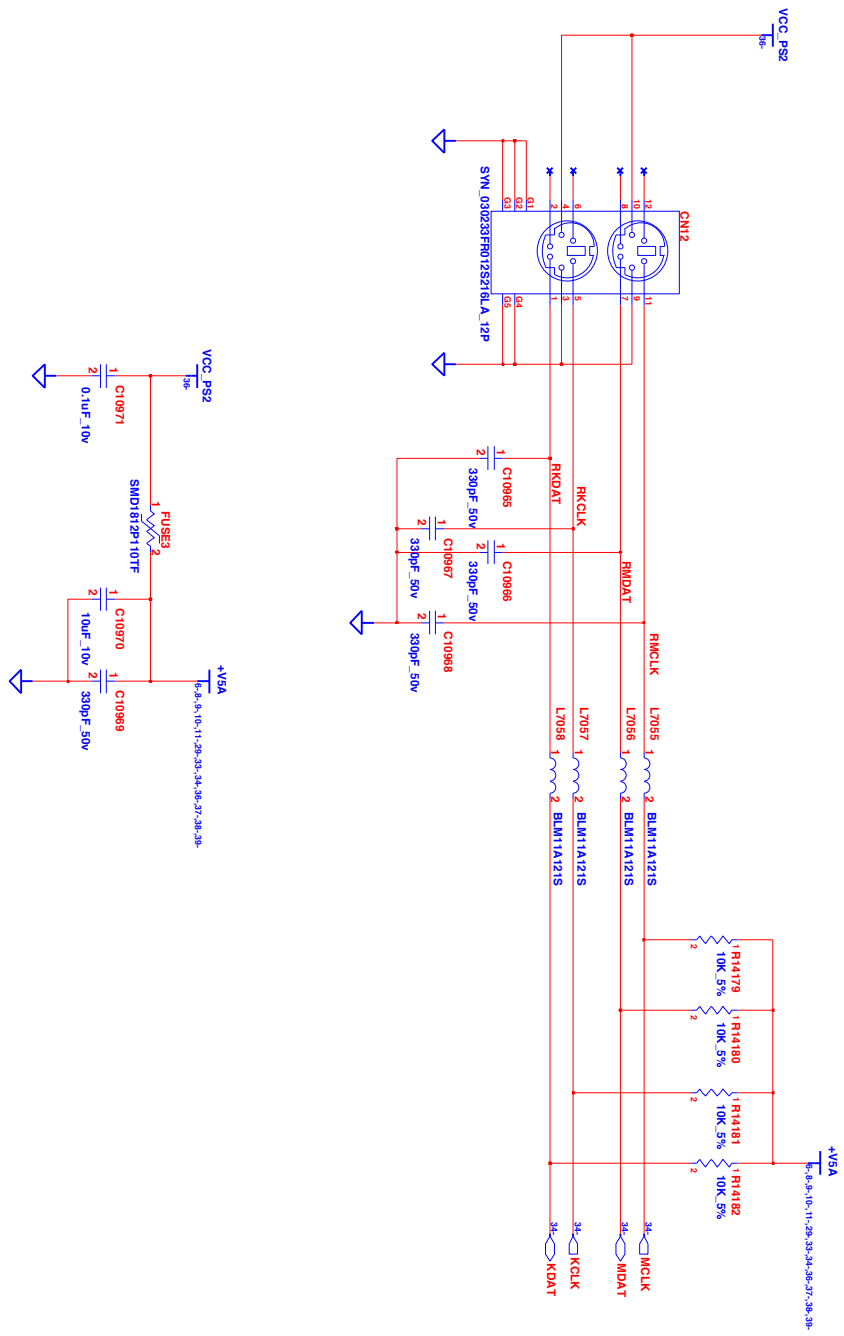
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A3	08	M-11 N-	YK

AS	CS	Model No	AO
SHEET 35 OF 40			

Category	33	01	49
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PS/2



INVENTEC

TITLE: M3

SIZE CODE: PS/2 CONN.

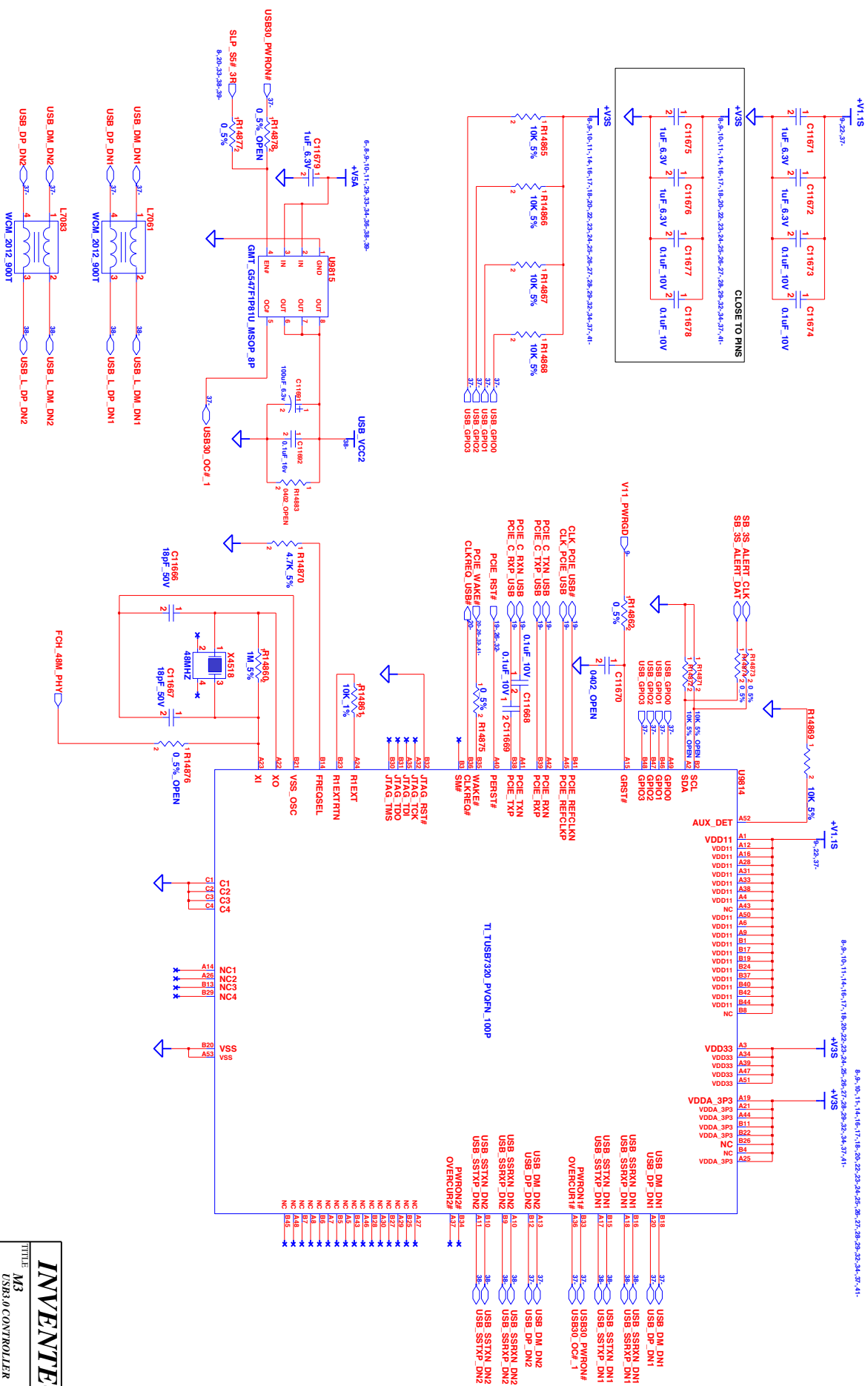
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DATE: 21-Aug-2010

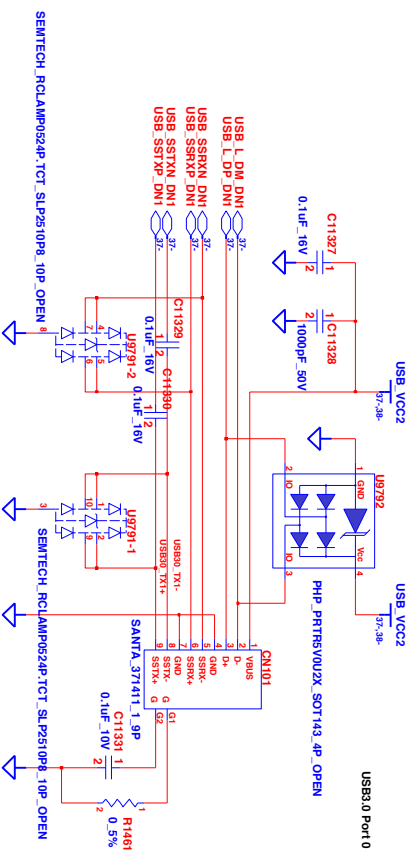
BY: HMA

CHANGED BY: HMA

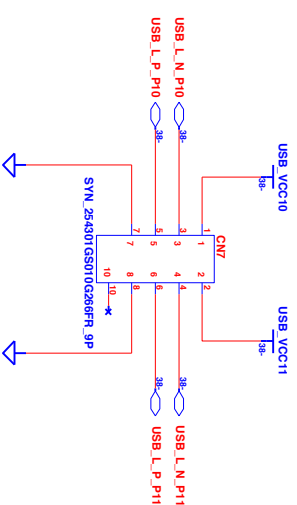
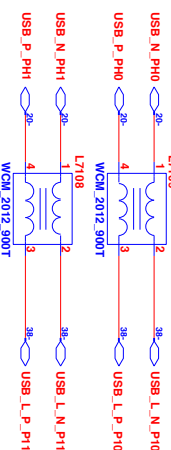
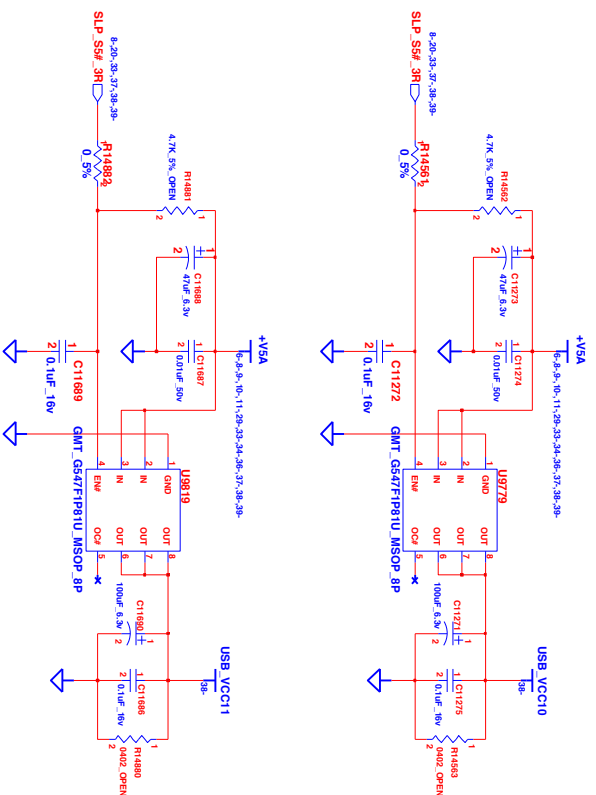
USB3.0 CONTROLLER



DUAL USB 3.0 CONN



USB HEADER



INVENTEC

M3

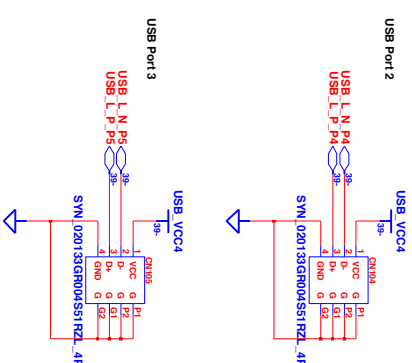
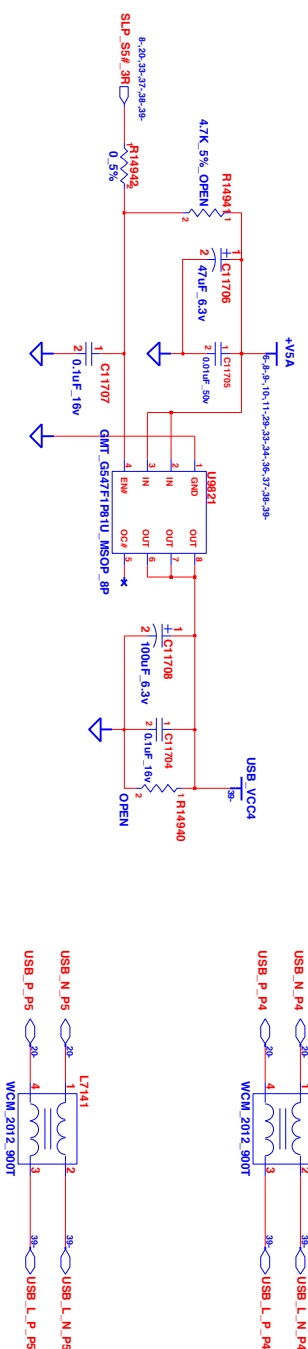
DUAL USB3.0 CONN/ USB HEADER

SIZE CODE DOC NUMBER REV

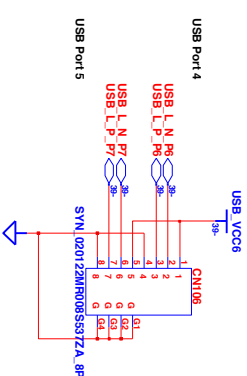
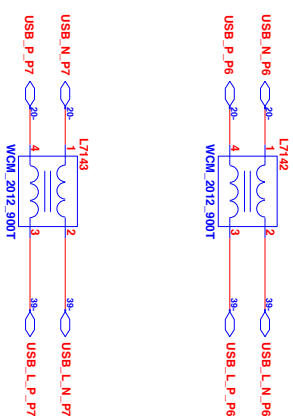
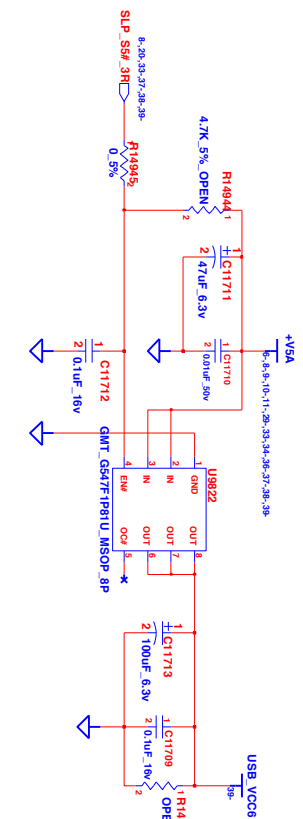
A3 CS Model No

SHRHT 38 OF 49

USB CONN



VERTICAL USB



INVENTEC

TITLE: **M3**

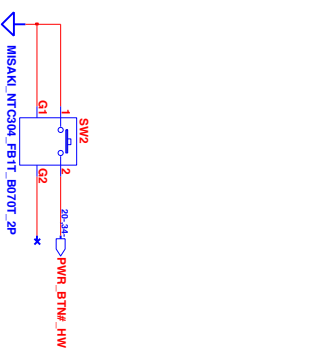
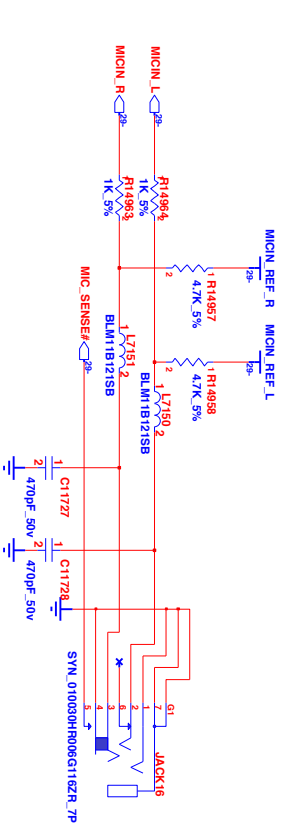
SIZE: **CODE**

REV: **CS**

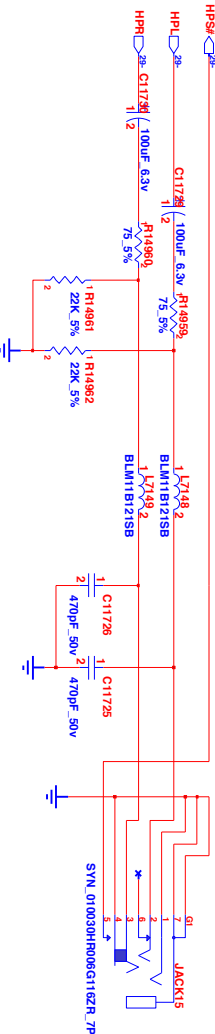
SYNTH: **39**

DATE: **21-Aug-2010**

REV: **101**

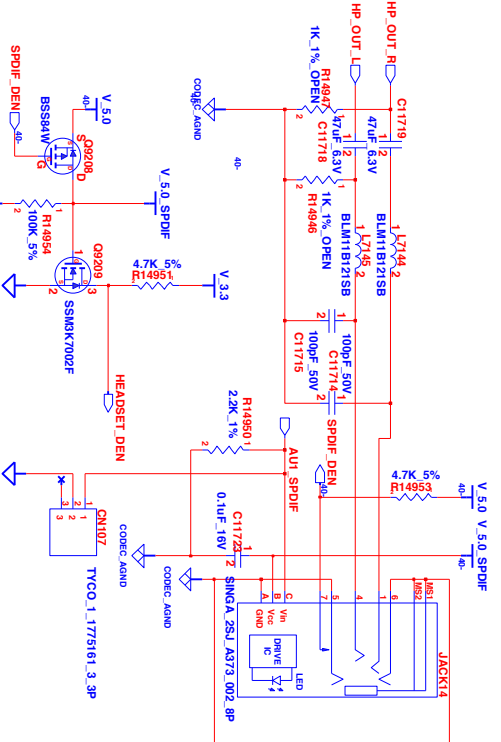
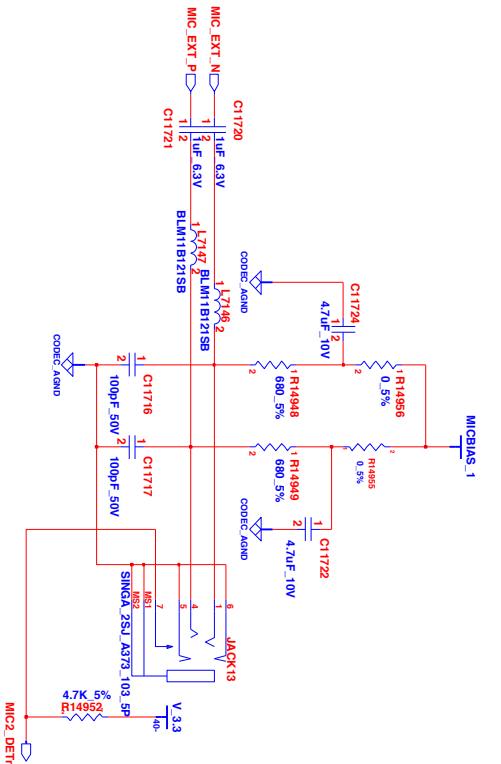
[illegible]

The schematic shows the HPSM power supply circuit. It starts with an input labeled "HPSM". The signal passes through a series of components: a capacitor C11726 (100nF, 6.3V), a resistor R14989 (75.5%), and another capacitor C11726 (100nF, 6.3V). This is followed by a diode bridge rectifier (BLMT1B121SB) and a filter capacitor C11725 (470pF, 50V). The output is connected to a terminal block labeled "JACK15" which has pins 1 through 7. A note indicates that the output voltage is 5V, 0.0003mH006G1f62R_7P.



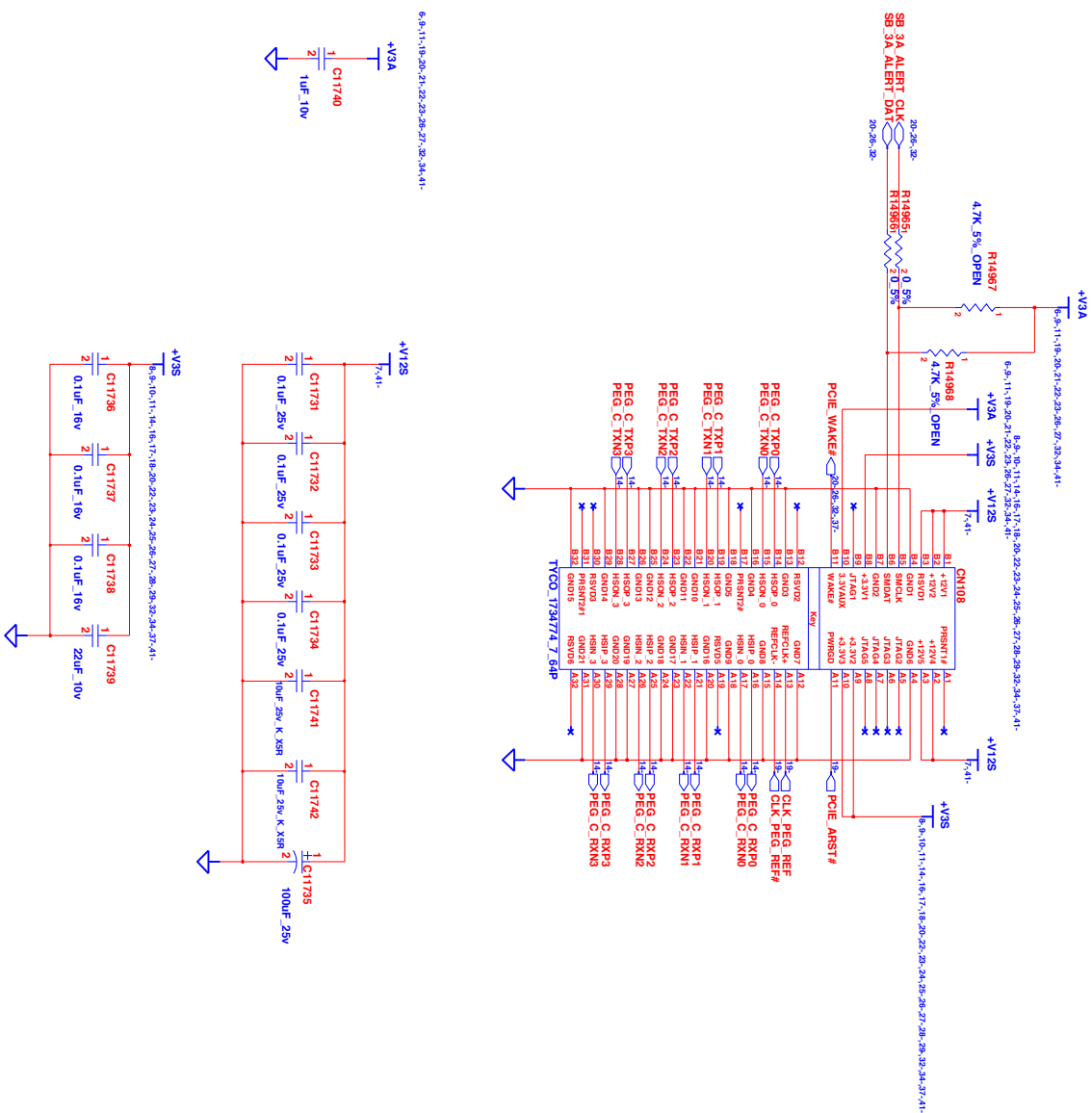
The schematic diagram illustrates the internal circuitry of the MIC215AS-1 audio amplifier. Key components and their connections are as follows:

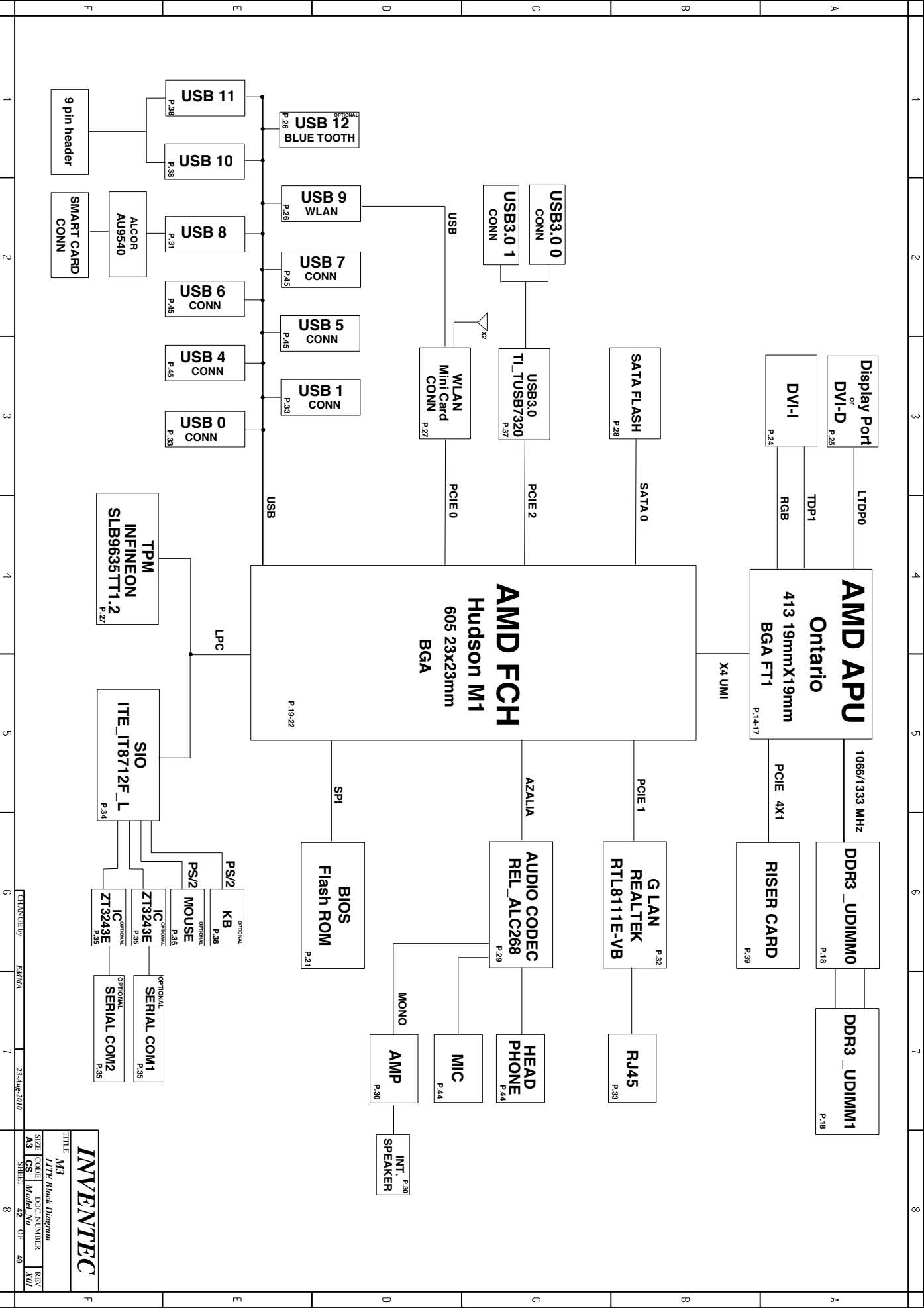
- Input Stage:** The MIC2 DET input is connected to a 4.7K 5% resistor (R14952) and a 100pF 50V capacitor (C11717). The output of this stage is connected to the MIC215AS-1 IC.
- Pre-amplifier Stage:** The MIC215AS-1 IC is connected to a 100pF 50V capacitor (C11716) and a 100pF 50V capacitor (C11717). The output of this stage is connected to the MIC215AS-1 IC.
- Power Amplifier Stage:** The MIC215AS-1 IC is connected to a 100pF 50V capacitor (C11716) and a 100pF 50V capacitor (C11717). The output of this stage is connected to the MIC215AS-1 IC.
- Output Stage:** The MIC215AS-1 IC is connected to a 100pF 50V capacitor (C11716) and a 100pF 50V capacitor (C11717). The output of this stage is connected to the MIC215AS-1 IC.



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RISERCARD CONN





[illegible]

[illegible]

